REMARKS

Claims 1-4, all the claims pending in the application, stand rejected. Claim 1 has been amended. Additional dependent claims 5-7 have been added.

Claim Rejections - 35 U.S.C. § 103

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Roza (6,795,001) in view of Dasgupta (6,529,077). This rejection is traversed for at least the following reasons.

The present invention concerns an improvement to a post filter for a delta sigma modulator used in digital signal processing for mobile telephones, PDAs, etc. The use of such filters at the output a delta signal modulator is known and a prior art approach is illustrated in Fig. 2 of the present application. However, this approach encounters problems with thermal noise, as explained at page 3 with regard to the filter 4 in Fig. 2. A similar problem exists where a FIR filter 4 is used that couples the output of the delta sigma modulator 2 to a multi stage flip-flop S, where each stage (F_1-F_n) being coupled to a corresponding MOS transistor pairs T_1, T1'-T_n, Tn'. The transistor pairs are coupled at their outputs to common resistors 7a-7b, which are used to convert currents into voltages. In this way, voltages according to the FIR filter coefficients may be obtained. The combined voltages are added and output to a circuit 5 configured with a full pass filter.

The present invention improves upon this arrangement. In an exemplary but non-limiting embodiment that incorporates the invention, Applicant has provided a constant current sources 8a, 8b in place of the resistors 7a, 7b so that the MOS transistors T1, T1'-Tn, Tn- control the conduction of <u>currents</u> from the constant current sources on the basis of the Q output and inverted Q output of each of the flip/flops (F1-Fn) in Fig. 1. In this manner, the <u>current</u> outputs from the constant current sources are weighted according to the filter coefficients of the FIR filter, added and outputted. Thus, a first improvement over the conventional design of Fig. 3 is that <u>currents</u> rather than <u>voltages</u> are weighted, added and output from the FIR filter.

Since the output is a <u>current</u>, the invention includes as a second feature a current/voltage conversion. In an exemplary embodiment, unit 6 is composed of a full differential operational

amplifier 6a and feedback resistor 6b, 6b connected in reverse polarity to the input and output of the differential amplifier 6a. This dual output is coupled to a single conversion operational amplifier 5a, of the type known in the conventional art, as illustrated in Fig. 3.

Because of the use of the constant current source, rather than resistors, for a current-to-voltage conversion, thermal noise provided by the resistors is avoided. Further, the use of a full differential operational amplifier 6a in the current-to-voltage conversion unit will remove common mode noises since the outputs from the FIR 4 are differentially inputted to a full differential operational amplifier.

These features of the invention are set forth in claims 1-4. Claim 1 specifically defines the output filter as comprising a FIR filter, which outputs data from a plurality of cascaded delay elements and controls current from a current source to obtain weighted currents according to the filter characteristic, adds the currents and outputs the results. The claim states that the current source is a constant current source. Dependent claims 2-4 specify a current-to-voltage conversion unit (Claim 2) and a single differential conversion operational amplifier (Claim 3).

Roza

The Examiner looks to Roza for a teaching of an output filter for a delta sigma modulator that comprises an FIR low pass filter, as illustrated in Fig. 1. The illustrated FIR filter comprises plural delay units C_1-C_n, each unit operative to generate a respective positive spike f which is then applied to a "divider by 2" latch E_1, which constitute an output tap O_1 of the delay line. The number of output taps is given by the required order of the filter. Respective switches S_1-S_n provide a multiplication with a weighting factor provided by weighting currents from current sources J_1-J_n [in the figure $I1$-I_n]. The switch weighting currents are added together to obtain the filter output signal.

An important difference is that Roza does not teach the conversion of the current into a voltage, using a current-to-voltage conversion unit. Moreover, Roza does not teach use of feedback resistors and a full differential operational amplifier. Indeed, Roza makes no disclosure of the processing of the output current from the filter illustrated in Fig. 1. Thus, the claims would be patentable over Roza taken alone.

Dasgupta

The Examiner cites Dasgupta for a teaching of an operational amplifier in Fig. 3 that receives two inputs N1, N2 and provides a single output that is subsequently divided into two currents that are converted to voltages by voltage-to-current converters VI1 and VI2, as explained at col. 7, line 24. However, there is no teaching or suggestion in either Roza or Dasgupta as to why one of ordinary skill would apply the operational amplifier arrangement of Dasgupta (particularly Fig. 4) to a pair of current-to-voltage converters. Indeed, only a single output is required from the FIR filter and there is no need for generating to such outputs. Finally, the output illustrated in Dasgupta is not provided to a single differential conversion operational amplifier, as claimed.

In short, the Examiner appears to be using hindsight to combine features of two references in order to arrive at the claimed invention, as first disclosed by the Applicant.

Applicant notes that claim 1 uses a narrative style and may not have clearly conveyed the structure of the invention, to the extent that constant current sources are being used. Accordingly, Applicant has amended claim 1 so that it clearly sets forth the use of a common constant current source at the output of the plural cascaded delay elements. Other amendments have been made to provide proper antecedent basis for claim terms.

Further, Applicant has added new claims 5-7 which add additional detail with regard to the placement of the constant current source and the individual transistor stages.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Amendment under 37 C.F.R. § 1.111
Application No. 10/730,928

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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